REMARKS/DISCUSSION OF ISSUES

By this Amendment, Applicant amends claim 1 for grammatical accuracy. Accordingly, claims 1-7 are pending in the application.

Reexamination and reconsideration are respectfully requested in view of the following Remarks.

35 U.S.C. § 112

The Office Action rejects claims 1-6 under 35 U.S.C. § 112.

Applicant respectfully submits that the amendment to claim 1 renders this rejection moot.

Accordingly, Applicant respectfully requests that the rejection of claims 1-6 under 35 U.S.C. § 112 be withdrawn.

35 U.S.C. § 102

The Office Action rejects claims 1-7 under 35 U.S.C. § 102 over Narayanan et al. U.S. Patent 6,081,913 ("Narayanan").

Applicant respectfully traverses these rejections for at least the following reasons.

Claim 1

Applicant respectfully submits that Narayanan actually does not disclose ***ANY*** of the three elements recited in claim 1!!

Among other things, the circuit of claim 1 includes components that operate asynchronously of one another.

Applicant respectfully submits that Narayanan does not disclose the recited components that operate asynchronously of one another.

The Office Action cites "logic circuitry 501" (illustrated as an empty "cloud") of FIG. 5 of Narayanan as supposedly corresponding to the recited components that operate asynchronously of one another.

Unfortunately, the Office Action does not cite even one line of text anywhere in Narayanan that discloses that logic circuitry 501 in Narayanan includes ***any***

components that operate asynchronously of one another. The undersigned attorney has reviewed Narayanan and does not see any such disclosure anywhere in Narayanan.

So, for at least this reason, Narayanan does not disclose the circuit of claim 1.

Also among other things, the circuit of claim 1 includes an interface element, the interface element having an output and at least two inputs, each input coupled to a respective one of the components, the interface element supplying a logic output signal that is a logical function of signals at the inputs, dependent on the relative timing with respect to each other of the signals at the inputs.

Applicant respectfully submits that Narayanan does not disclose the recited interface circuit.

The Office Action cites "gating circuit 201" of FIGs. 2, 3, 5 and 7 of Narayanan as supposedly corresponding to the recited interface element.

Unfortunately, the Office Action does not cite even one line of text anywhere in Narayanan that discloses that gating circuit 201 in Narayanan supplies a logic output signal that is a logical function of signals (plural) at the inputs. Indeed, it appears quite evident from FIG. 3 that each output signal of gating circuit 201 is only a function of a corresponding one input signal! (i.e., signal 105 is only a function of signal 305, and signal 103 is only a function of signal 307). Furthermore, none of the output signals from gating circuit 201 in Narayanan are "dependent on the relative timing with respect to each other of the signals at the inputs."

So, for at least this additional reason, Narayanan does not disclose the circuit of claim 1.

Further still, among other things, the circuit of claim 1 also includes a delay element coupled to cause a relative delay between the time intervals after which the signals at the inputs affect the interface element.

Applicant respectfully submits that Narayanan does not disclose the recited delay element.

The Office Action cites "mutual exclusivity circuit 701" of FIG. 7 of Narayanan as supposedly corresponding to the recited delay element.

Although the Office Action provides a lot of discussion about internal components (e.g., elements 903, 905, 907) of mutual exclusivity circuit 701, and about the scan chain 107, but no where does the Office Action simply state that mutual exclusivity circuit 701 causes a relative delay between the time intervals after which the signals (e.g., 305 and 307 in FIG. 3) at the inputs affect the interface element (e.g., gate circuit 201). The undersigned attorney has reviewed Narayanan and does not see any such disclosure anywhere in Narayanan.

So, for at least this additional reason, Narayanan does not disclose the circuit of claim 1.

Accordingly, for at least these reasons, Applicant respectfully submits that claim 1 is clearly patentable over Narayanan.

Claims 2-6

Claims 2-6 all depend from claim 1 and are deemed patentable for at least the reasons set forth above with respect to claim 1, and also for the various additional novel features recited therein.

Claim 7

Among other things, the method of claim 7 includes causing a difference between the time intervals after which the test signal source affects different ones of the signals at the inputs to an interface element, where the inputs are each coupled to a respective one of components that operate asynchronously of one another.

Again, the Office Action has cited gating circuit 201 of Narayanan as supposedly corresponding to the recited interface element, and mutual exclusivity circuit 701 Narayanan as supposedly causing a difference between the time intervals after which a test signal source affects different ones of the signals at the inputs (e.g., inputs 305 and 307) to gating circuit 201.

As explained above with respect to claim 1, Applicant respectfully submits that Narayanan does not disclose any such features.

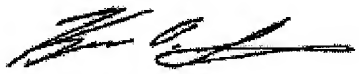
Accordingly, for at least these reasons, Applicant respectfully submits that claim 7 is patentable over Narayanan.

CONCLUSION

In view of the foregoing explanations, Applicant respectfully requests that the Examiner reconsider and reexamine the present application, allow claims 1-7 and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283.0720 to discuss these matters.

Respectfully submitted,

VOLENTINE & WHITT



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